

WIRELESS TEST SYSTEM

BACKGROUND

[0001] Although this invention is generally applicable to test systems and methods in general, it is particularly suited for semiconductor device testing.

[0002] As known, semiconductor devices are typically manufactured many at a time as "dice" on a semiconductor wafer, after which the dice are further processed before being shipped to customers or installed in various products. That further processing may take many forms.

[0003] In perhaps the most common post-manufacture processing, the dice are probed while still in wafer form and initial testing is performed on each die. Thereafter, the dice are singulated from the wafer, and the dice that passed the initial probe testing are packaged, burned in, and further tested. In another common process, the dice are not packaged after being singulated from the wafer but are further tested and often burned in to produce "known good dice," which are unpackaged dice that have been fully tested. In more advanced processes, the dice are burned in and fully tested while in wafer form. In all of these exemplary post-manufacture processes, as well as other scenarios in which electronic devices of any kind are tested, there is a need to control testing and/or exercising of the dice or other electronic devices.

BRIEF SUMMARY

[0004] The present invention relates generally to test systems and methods. In an embodiment of the invention, one or more testers wirelessly communicate with one or more test stations. The wireless communication may include transmission of test commands, test vectors, test results, and/or messages.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0005] Figure 1 illustrates a block diagram of major elements of an exemplary test system.

[0006] Figure 2 illustrates an exemplary process that may be run by the controller 140 of Figure 1.

[0007] Figure 3 illustrates an exemplary process that may be run by the controllers 160 of Figure 1.

[0008] Figure 4 illustrates an exemplary detailed implementation of steps 204 and 206 of Figure 2.

[0009] Figure 5 illustrates an exemplary detailed implementation of steps 304 and 306 of Figure 3.

[0010] Figure 6 illustrates a block diagram of major elements of another exemplary test system.

[0011] Figure 7 illustrates an exemplary detailed implementation of steps 204 and 206 of Figure 2 run on the controller 140 of Tester I in Figure 6.

[0012] Figure 8 illustrates an exemplary detailed implementation of steps 204 and 206 of Figure 2 run on the controller 140 of Tester II in Figure 6.

[0013] Figure 9 illustrates a block diagram of major elements of yet another exemplary test system.

[0014] Figure 10 illustrates an exemplary detailed implementation of steps 204 and 206 of Figure 2 run on the controller 140 of Tester I in Figure 9.

[0015] Figure 11 illustrates an exemplary detailed implementation of steps 204 and 206 of Figure 2 run on the controller 140 of Tester II in Figure 9.

[0016] Figure 12 illustrates an exemplary detailed implementation of steps 304 and 306 of Figure 2 run on the controllers 160 in Figure 9.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0017] The present invention relates generally to test systems and methods. This specification describes exemplary embodiments and applications of the invention. The invention, however, is not limited to these exemplary embodiments and applications or to the manner in which the exemplary embodiments and applications operate or are described herein.

[0018] Figure 1 illustrates an exemplary test system 100. The system 100 includes a tester 102 and three test stations: test station A 104a, test station B 104b, and test station C 104c, although more testers and fewer or more test stations may be used. Tester 102 includes wireless

transceiver 106, and test stations 104a-104c also each include a wireless transceiver 110.

Optionally, tester 102 may include a microprocessor-based control system 140. A block diagram of the basic components of an exemplary microprocessor-based control system 140 are shown in Figure 1, which includes a microprocessor 142, a main memory 148, a program memory 150, a general input/output block 144, and a transceiver input/output block 146. Each test station 104a-104c may include a similar microprocessor-based control system 160, with similar elements, including a microprocessor 162, a main memory 168, a program memory 170, a general input/output block 164, and a transceiver input/output block 166.

[0019] Test station A 104a, test station B 104b, and test station C 104c each includes one or more electronic devices to be tested. In the example shown in Figure 1, all of the test stations 104a, 104b, 104c are probers for probing a semiconductor wafer 114 comprising a plurality of dice 116a, 116b, 116c. Thus, the electronic device to be tested in each of test stations 104a-104c is a wafer 114 or more specifically the dice 116a-116c. (Three dice 116a, 116b, 116c per wafer 114 are shown in Figure 1 for simplicity. Typically, many more dice are fabricated on a wafer.)

[0020] As known, such probers typically include a moveable chuck 120, a probe card 108 having probes 112 for contacting pads 118 on one or more of the dice 116a, 116b, 116c. Test stations 104a, 104b, 104c, however, need not be probers but may be any type of apparatus in which an electronic device is tested or exercised. Nonlimiting examples include an apparatus comprising sockets, test probes, or load boards for holding packaged or unpackaged (singulated) semiconductor dice during testing and/or burn in. Another example is an apparatus for testing multi-chip modules. (The term "testing," as used herein, is intended to cover broadly any form of exercising an electronic device that is part of a larger process of determining the usability, functionality, performance, or reliability of the electronic device. Thus, for example, the term "testing" includes exercising a semiconductor device during burn in regardless of whether the device is monitored or analyzed during the exercising.) Tester 102 controls testing of the electronic devices 114.

[0021] Transceivers 106 and 110 allow the tester 102 and the test stations 104a-104c to communicate wirelessly. Thus, although tester 102 and test stations 104a-104c may be located near each other, each may be located remotely from the others. Element 122 in Figure 1 represents an optional physical separation between the tester 102 and the test stations 104a-104c.

Thus, tester 102, on one hand, and test stations 104a-104c, on the other hand, may be located in different rooms, different buildings, or even different geographical locations. The wireless link between the tester 102 and each of the test stations 104a-104c may be any type of wireless link, including without limitation any type of optical or radio signal link and may include such intermediate elements as repeaters and/or communication satellites. Indeed, the tester 102 and its transceiver 106 may be remotely located one from another with a communication network, such as a local area network, wide area network, or metropolitan area network or the Internet, between them. Although not shown in Figure 1, test stations 104a-104c may also be physically separated or located remotely one from another.

[0022] Figure 2 illustrates basic operation of the tester 102, and Figure 3 illustrates basic operation of a test station 104. (Reference to “104” without specifying “a,” “b,” or “c” refers to any one or more of the test stations.) At step 202, the tester 102 is initialized, and at step 302 a test station is initialized. At step 204, the tester 102 sends wirelessly test data to a test station 104, and at step 304, the test station 104 tests an electronic device 114 in accordance with the test data. At step 306, the test station 104 transmits wirelessly results of the testing to the tester 102, which is received by the tester at step 206.

[0023] As one option, the processes shown in Figure 2 may be implemented in the tester 102 as software (including firmware or microcode) stored in program memory 150 and executed by microprocessor 142. Similarly, the process illustrated in Figure 3 may be implemented in a test station 104 as software stored in program memory 170 and executed by microprocessor 162. In the tester 102, data to be transmitted by the transceiver 106 and data received via the transceiver 106 may be output or input through the transceiver input/output block 146. Other data may be input or output through the general input/output block 144. The general input/output block 164 and the transceiver input/output block 166 in a test station's microprocessor-based controller 160 may be generally similar to like elements in the tester's controller 140.

[0024] The test data sent by the tester 102 to a test station 104 may be in any format recognizable by the test station. As one example, the test data may be test vectors that include both the data to be written to the electronic device under test 114 and an identification of the probes through which the test data is to be written. In such case, the test station 104 simply places data on the probes as specified by the test vectors. As another example of a format for the

test data, the test data may comprise commands that cause a test station 104 to generate test vectors for testing a die 116a-116c. The results data transmitted by a test station 104 back to the tester 102 may likewise be in any format recognizable by the tester 102, which may range from raw data generated by the die 116a-116c to data representing an analysis or summary of the response of the die 116a-116c to the test data.

[0025] Figure 4 illustrates an exemplary detailed implementation of steps 204 and 206 from Figure 2, and Figure 5 illustrates a corresponding implementation of steps 304 and 306 from Figure 3. The exemplary processes of Figures 4 and 5 will be discussed with respect to the test system 100 shown in Figure 1. As will be seen, the process of Figure 4 causes the tester 102 to initiate testing at the test stations 104a-104c, after which the tester 102 waits for messages from the test stations 104a-104c indicating that testing is completed. Upon receiving such a message, the tester 102 requests transfer of the test results data.

[0026] For purposes of illustration, it will be assumed that test station A 104a and test station B 104b are initialized at step 302 of Figure 3. This initialization may include such things as loading wafers 114 to be tested into test station A 104a and test station B 104b. Initialization may also include loading data into the main memory 168 of the microprocessor-based control system 160 in each of test station A 104a and test station B 104b. If the test data to be received from the tester 102 comprise test commands, a command table for decoding the commands may also be loaded into the main memory 168 of each of the test stations 104a and 104b. To complete initialization, each test station 104a and 104b sends a request to the tester 102 to be brought on line for testing. The request may include data both identifying the test station and the type of wafer loaded into the test station.

[0027] In the mean time, the tester 102 is also initialized at step 202 of Figure 2. Initialization of the tester 102 may include such things as loading a list of wafer types and tests to be run on each wafer type into the main memory 148 of the microprocessor-based control system 140 in the tester 102. As mentioned above, in this example, it is assumed that the test sequences are defined by one or a series of test commands. To complete initialization, the tester 102 brings all test stations 104 from which a message requesting to be brought on line has been received. This may be done, for example, by creating a list of the test stations to be brought on line and the

wafer type in each test station, and storing the list in the main memory 148 of the controller 140 in the tester 102.

[0028] After initialization of both the tester 102 and test station A 104a and test station B 104b, the tester 102 is ready to begin executing the process illustrated in Figure 4, and each on-line test station—test station A 104a and test station B 104b—is ready to begin executing the process shown in Figure 5. (Note that in this example, test station C 104c was not initialized and brought on line for testing.)

[0029] As shown in Figure 4, the tester 102 selects a test station at step 402. The selected test station may be any of the on-line test stations as listed in the tester's main memory 148. In this example, there are two test stations—test station A 104a and test station B 104b—listed as on-line in the tester's main memory 148, and the tester 102 selects test station A 104a at step 402. At step 404, the tester 102 initiates testing of the wafer 114 in the selected test station 104a. As mentioned above, in this example, the tester 102 does so by transmitting wirelessly to the selected test station—test station A 104a—a test command or a series of test commands. To do so, the tester 102 looks in its main memory 148 at the type of wafer in the selected test station 104a, and then retrieves, also from its main memory 148, the test command or series of test commands for that wafer type. The test command or commands define the test(s) to be performed on the dice of that wafer type. Step 404 may also include setting a flag in the tester's main memory 148 indicating that testing is underway in the selected tester 104a.

[0030] After initiating testing at the selected test station 104a at step 404, the tester 102 determines at step 406 whether it has received any messages. If not, the tester selects another of the on-line testers at step 408. The tester 102 may do so by searching the list of on-line test stations in the tester's main memory 148 for a test station where testing is neither underway nor completed. In this example, the tester 102 selects test station B 104b at step 408 and then repeats step 404, initiating testing in the newly selected test station B 104b by wirelessly transmitting a test command or series of test commands, as described above. In this example, there are only two test stations on line—test station A 104a, and test station B 104b. In other examples involving more on-line test stations, this process would continue to be repeated.

[0031] During this process, if a message is received, execution branches at 406 so that the message is decoded and any necessary action taken. If the message is from a test station 116a-

116c indicating that testing at that test station 104 has completed (see step 410), then the tester 102 processes the results of the testing at step 412. Processing the test results (step 412) may include such things as sending a message to the test station requesting transmission of the test results. (Alternatively, if the test results were transmitted with the message from the test station, the tester 102 reads the test results from an internal buffer (not shown).) Step 412 may also include additional actions, such as setting a flag in the tester's main memory 148 indicating that testing has completed at that test station. If, as shown in Figure 1, the test station contacts less than all of the dice 116a-116c on the wafer 114 being tested, step 412 may include causing the test station to reposition the wafer 114 to contact an as yet untested die or dice. After processing the test results at step 412, the process of Figure 4 repeats step 408 of selecting a new test station, from which the process beginning with step 404 is repeated as necessary to initiate testing at the test stations.

[0032] If the message detected at step 406 was a request from a new test station to be brought on line or a request from an on-line test station to be taken off line (see step 414), then the new test station is brought on line at step 416 or the on-line test station is brought off line at step 416. Bringing a new test station on line may include such things as adding the new test station's identifier and wafer type to the list of on-line test stations stored in the tester's main memory 148. Likewise, taking an on-line test station off line may include such things as deleting the test station's identifier and wafer type from the same list.

[0033] In the example being discussed, only test station A 104a and test station B 104b were brought on line. While testing is occurring at those two test stations 104a, 104b, an operator may initialize test station C 104c by, among other things, loading a wafer 114 into test station C 104c. Test station C 104c may then send a request to the tester 102 to be brought on line. As discussed above, the tester 102 will then bring test station C 104c on line at step 416 of Figure 4. Once on line, test station C 104c will eventually be selected at step 408 and tests initiated at step 404.

[0034] As mentioned above, Figure 5 illustrates operation of each of the test stations 104 in response to messages sent by the tester 102 during operation of the process shown in Figure 4. As also mentioned above, Figure 5 illustrates an exemplary detailed implementation of steps 304 and 306 of Figure 3 and is therefore executed after the initialization step 302 of Figure 3. As shown in Figure 5, each on-line test station 104 waits for a message at step 501. If a message

containing a test command is received from the tester 102 (see steps 506, 510), then the test command is executed at step 512. The test command may be executed, for example, by finding the test command in a decode table stored in the test station's main memory 168 and taking the actions indicating in the decode table for the test command. As just one example, the decode table may contain a test vector or vectors that are to be written to the wafer 114. As another example, the test station 104 may generate commands that are sent to the dice 116a-116c and executed by self test circuitry on the dice (e.g., so called built-in-self-test circuitry). Execution of the test command may also include buffering the response data generated by the die being tested and sending a message to the tester 102 that testing is completed and response data is ready. If the message was a request from the tester 102 to send test results for testing that has completed (see step 514), then the test results (which may be buffered at the test station 104) are transmitted wirelessly to the tester at step 516. Alternatively, the test results may be stored and/or analyzed solely at the test station, and the results may be retrieved by other than the tester 102—e.g., an operator—from the test station 104.

[0035] Step 418 in Figure 4 and step 518 in Figure 5 illustrate other miscellaneous actions that may be taken by the tester 102 or a test station 104. Such other actions may include ending the process, handling errors, etc. In addition, provisions may be made in each process for processing multiple messages. These and other modifications and additions to the processes shown in Figures 4 and 5 are within the skill of the ordinary practitioner in the field and need not be discussed.

[0036] Figure 6 illustrates another exemplary test system 600. As shown, test system 600 also includes three test stations: test station A 604a, test station B 104b, and test station C 104c, although fewer or more could be used. In this example, each test station 604a-604c includes a load board 608 with sockets 612 for receiving singulated dice 616a, 616b. Each load board also includes a transceiver 610 and internal wiring (not shown) for carrying test signals and response data to and from the dice 616a, 616b. Each test station 604a-604c also includes a controller 160, which may be generally similar to controller 160 discussed above with respect to Figure 1.

[0037] Test system 600 also includes two testers: tester I 602a and tester II 602b. Again, however, fewer or more testers may be used. Each tester 602 includes a transceiver 606 and a controller 140, which may also be generally similar to controller 140 discussed above with

respect to Figure 1. A communication link 626 interconnects tester I 602a and tester II 602b and also connects to storage unit 624. Communication link 626 may be any type of electronic communication device, including without limitation a cable, a wireless link, a computer network, etc. Like 122 in Figure 1, element 622 represents optional physical separation.

[0038] In this example, tester I 602a causes a first functional test (test 1) to be performed on the dice 616a, 616b, and tester II 602b causes a second functional test (test 2) to be performed on the same dice. Thus, full testing of the dice 616a, 616b, in this example, includes both test 1 and test 2. For example, test 1 may be a fast functional test, and test 2 may be a longer, more exacting functional test. More than two sequential tests may be run on the dice 116a, 116b, and such tests could include exercise during burn in.

[0039] The processes shown in Figures 2 and 3 may also be run on the testers 602a, 602b and test stations 604a-604c of Figure 6. That is, the process shown in Figure 2 may be run on each of the testers 602a, 602b, and the process shown in Figure 3 may be run on each of the test stations 604a-604c.

[0040] Figures 7 and 8 illustrate an exemplary detailed implementation of steps 204 and 206 from Figure 2 that may be run on tester I 602a and tester II 602b, respectively. The process of Figure 5, discussed above, may be implemented on each of the test stations 604a-604c. As will be seen, in the process of Figure 7, tester I 602a initiates a first test (test 1) at the test stations 604a-604c, after which tester I 602a waits for a message from each test station indicating that test 1 has completed at that test station. Upon receiving such a message from a particular test station, tester I 602a requests transfer of the results of test 1 from that particular test station, and tester I 602a sends a message to tester II 602b indicating that test 1 has completed at that test station. Upon receiving this message from tester I 602a, tester II 602b initiates test 2 at that particular test station, and then waits for a message from that test station that test 2 has been completed, after which tester 2 602b requests the results of test 2 from the test station. Both testers 602a, 602b may store the results of the tests in the storage device 624.

[0041] For purposes of illustration, it will be assumed that test station A 604a, test station B 604b, and test station C 604c are all initialized at step 302 of Figure 3. This initialization may be generally similar to the initialization of test station A 104a and test station B 104b of Figure 1 as described above with respect to Figures 3-5. For example, initialization of test station A 604a,

test station B, 604b, and test station C 604c may include such things as securing dice to be tested 616a, 616b to load boards 608, and placing a load board in each test station. Initialization data may also be loaded into the main memory 168 of the microprocessor-based control system 160 in each test station 604a-604c. If the test data to be received from the testers 602a, 602b comprise commands, a command table for decoding the commands may also be loaded into the main memory 168 of each of the test stations 604a-604c. To complete initialization, each test station 604a-604c sends a request to tester I 602a to be brought on line for testing. The request may include data both identifying the test station and the type of dice to be tested at the test station.

[0042] In the mean time, tester I 602a and tester II 602b are also initialized at step 202 of Figure 2. Initialization of the testers 602a, 602b may also be similar to the initialization of tester 102 described above with respect to Figures 2, 4, and 5. For example, initialization in each tester 602a, 602b may include such things as loading a list of dice types and test sequences to be run on each dice type into the main memory 148 of the microprocessor-based control system 140 in each tester 602a, 602b. As mentioned above, in this example, it is assumed that the test sequences are defined by one or a series of test commands. To complete initialization, tester I 602a brings on line all test stations from which a message requesting to be brought on line has been received. This may be done, for example, by creating a list of the test stations to be brought on line and the dice type in each test station, and storing the list in the main memory 148 of the microprocessor-based control system 140 in tester I 602a.

[0043] After initialization of the testers 602a, 602b and the test stations 604a-604c, tester I 602a is ready to begin executing the process illustrated in Figure 7; tester II 602b is ready to begin executing the process illustrated in Figure 8; and each on-line test station—test station A 604a, test station B, 604b, and test station C 604c—is ready to begin executing the process shown in Figure 5.

[0044] As shown in Figure 7, tester I 602a selects a test station at step 702. The selected test station may be any of the on-line test stations listed in the main memory 148 of tester I 602a. For illustration purposes in this example, there are three test stations—test station A 604a, test station B 604b, and test station C 604c—listed as on-line in the main memory 168 of tester I 602a, and tester I 602a selects test station A 604a at step 702. At step 704, tester I 702 initiates

test 1 on the dice 616a, 616b at the selected test station—test station A 604a. As mentioned above, in this example, tester I 602a does so by transmitting wirelessly the selected test station 604a one or a series of test commands that define test 1. Step 704 may also include setting a flag in the main memory 148 of Tester I 602a indicating that testing is underway at the selected test station—test station A 604a.

[0045] After initiating test 1 at the selected test station—test station A 604a—at step 704, tester I 602a determines at step 706 whether it has received any messages. If not, tester I 602a selects another of the on-line testers at step 708, which may be accomplished generally as described above with respect to Figure 4. In this example, tester I 602a selects test station B 604b at step 708 and then repeats step 704, initiating test 1 on the dice 616a, 616b in the newly selected test station, which is now test station B 604b.

[0046] In this example, it is assumed that test station A 604a completes test 1 and sends a message indicating as much to tester I 602a shortly after tester I 602a initiates test 1 at test station B 604b. Thus, at the next pass through the process of Figure 7, a message is detected at step 706, causing the process of Figure 7 to branch to step 710. Because the message indicates that test 1 has completed at test station A 602a, the process of Figure 7 branches to step 712, where tester I 602a processes the results of test 1 in test station 602a. Processing the results of test 1 (step 712) may include such things as sending a message to the test station requesting transmission of the results of test 1. (Alternatively, if the test results were transmitted with the message from the test station, tester I 602a reads the test results from an internal buffer (not shown).) Step 712 may also include additional actions, such as setting a flag in the main memory 148 of tester I 602a indicating that test 1 has been completed at that test station.

[0047] After processing at step 712 the test results of test 1 executed at test station A 604a, the process of Figure 7 sends a message to tester II 602b indicating that test 1 has completed at test station A (see step 713). As will be seen, this causes tester II 602b to initiate test 2 at test station A 604a. Thereafter, tester I 602a repeats step 708 and selects this time test station C 604c and repeats the process shown in Figure 7 at step 704, initiating test 1 at test station C 604c.

[0048] Referring now to Figure 8, which illustrates exemplary operation of tester II 602b, after initialization at step 202 of Figure 2 (as discussed above), tester II 602b waits for a message at step 801. Upon receiving the message from tester I 602a that test 1 has completed at test station

A 604a (see step 713 of Figure 7, as discussed above), tester II 602b takes the "yes" branches at steps 806 and 807 of Figure 8. At step 809, tester II 602b initiates test 2 at test station A 604a. Tester II 602b does so by wirelessly sending to test station A 604A a command or series of commands that define test 2. As test 1 finishes in each of the remaining test stations B 604b and C 604c, tester I 602a processes the results of test 1 at those test stations at step 712 of Figure 7 and sends a message at step 713 of Figure 7 to tester II 602b, indicating that test 1 has completed at each of those test stations. Tester II 602b then initiates test 2 in each of those test stations, per steps 806, 807, 809 of Figure 8. As test 2 completes at each of the test stations 604a-604c, each test station sends a message to tester II 604b. In response to each such message, tester II 604b processes the results of test 2 at that particular test station, per steps 806, 810, 812 of Figure 8. The step of processing test results at step 812 may be generally similar to step 412 of Figure 4 and step 712 of Figure 7.

[0049] During these processes, a new test station may send a message to tester I 602a requesting to be brought on line. Likewise, an on-line test station may send a message to tester I 602a requesting to be taken off line. Such requests are processed by tester I 602a at steps 714, 716 of Figure 7, and may be accomplished in a manner generally similar to step 416 of Figure 4 as described above. As just one example, when test 2 completes in test station A 602a, an operator may cause test station A 602a to be taken off line, replace the now fully tested dice 116a, 116b with new dice to be tested, and cause test station A 602a to be brought back on line, now as a new test station with dice to be tested. This may be accomplished by causing test station A 604a to send tester I 602a a message requesting to be taken off line, and then after loading a new wafer 114 to be tested into test station A 604a, causing test station A to send tester I 602a a message requesting to be brought on line.

[0050] It should be apparent that testers may also be brought on and off line. By strategically bringing testers and test stations on and off line as needed, a test system may be balanced for maximum data through put between tester and test stations and maximum testing efficiency.

[0051] Step 718 in Figure 7 and step 818 in Figure 8 illustrate other miscellaneous actions that may be taken by tester I 602a and tester II 602b, which may be generally similar to miscellaneous actions described above with respect to Figures 4 and 5.

[0052] Figure 9 illustrates another exemplary test system 900. Test system 900 also includes three test stations: test station A 904a, test station B 904b, and test station C 904c, although fewer or more may be used. In this example, each test station 904a-904c is a prober for probing an unsingulated semiconductor wafer 914 comprising a plurality of dice 916a-916d. (Again, four dice 916a-916d are shown for ease of illustration, but more or fewer may be present.) Such probers may be similar to the probers discussed above with respect to Figure 1 and may include such things as a probe card 908 with probes 912 for contacting pads 918 on wafer 914 and a chuck 920 for holding and moving wafer 914. Each test station 904a-904c also includes a transceiver 910 and a controller 160, which may be generally similar to transceiver 910 and a controller 160 as in Figure 1.

[0053] Test system 900 also includes two testers: tester I 902a and tester II 902b. Each tester includes a transceiver 906 and a controller 140, which may also be generally similar to controller 140 discussed above with respect to Figure 1. Similar to Figure 6, a communication link 926 interconnects tester I 902a and tester II 902b and also connects to storage unit 924. As discussed above with respect to Figure 6, communication link 926 may be any type of electronic communication link. Like element 122 in Figure 1 and element 622 in Figure 6 (both discussed above), element 922 represents an optional physical separation. In this example, probe card 908 is capable of contacting two dice at one time. Probe card 908 is shown in Figure 9 contacting dice 916a, 916b. Often a probe card will contact more than two dice, but two dice are shown in Figure 9 for ease of illustration.

[0054] In this example, rather than send test data in the form of test commands, Tester I 902a and Tester II 902b send test vectors to test stations 904a-904c. For purposes of this example, it is assumed that neither tester 902a, 902b has sufficient bandwidth to send enough test vectors to test both die 916a and die 916b at the same time. As will be seen, Tester I and Tester II both send the same test vectors to a particular test station 904. The test station 904 uses test vectors from one tester to test one of the dice and test vectors from the other tester to test the other die.

[0055] The general process shown in Figure 2 may also be run on the I 902a and tester II 902b of the test system 900 shown in Figure 9, and the general process shown in Figure 3 may be run on test station A 904a, test station B 904b, and test station C 904c.

[0056] Figure 10 illustrates an exemplary detailed implementation of steps 204 and 206 from Figure 2 that may be run in tester I 902a, and Figure 11 illustrates an exemplary detailed implementation of steps 204 and 206 from Figure 2 that may be run in tester II 902b. Figure 12 illustrates an exemplary detailed implementation of steps 304 and 306 from Figure 3 that may be run in each of test station A 904a, test station B 904b, and test station C 904c. As will be seen, in the processes of Figures 10 and 11, tester I 902a selects a test station having a wafer in need of testing and sends a message to tester II 902b. Tester I 902a then initiates testing of die 1 916a at the selected test station, and tester II 902b initiates testing of die 2 916b at the selected tester. Tester I 902a then continues to select test stations with wafers in need of testing, after which both testers continue to initiate testing of the dice at the selected test stations. As the various tests are completed, both testers collect the test results and store the results in the storage device 924. The testers 902a, 902b communicate with the test stations 904a, 904b, 904c wirelessly.

[0057] Again, for purposes of illustration, it will be assumed that test station A 904a, test station B 904b, and test station C 904c are initialized at step 302 of Figure 3. This initialization may be generally similar to the initialization of test stations 104a and 104b described above with respect to Figures 3-5. To complete initialization, each of test station A 904a, test station B 904b, and test station C 904c sends a request to tester I 902a to be brought on line for testing. The request may include data both identifying the test station and the type of wafer loaded into the test station.

[0058] In the mean time, tester I 902a and tester II 902b are also initialized at step 202 of Figure 2. Initialization of the testers 902a, 902b may also be similar to the initialization of tester 102 described above with respect to Figures 2, 4, and 5. To complete initialization, tester I 902a brings on line all test stations from which a message requesting to be brought on line has been received. This may be done, for example, by creating a list of the test stations to be brought on line and the wafer type in each test station, and storing the list in the main memory 148 of the microprocessor-based control system 140 of tester I 902a.

[0059] After initialization of the testers 902a, 902b and the test stations 904a-904c, tester I 902a is ready to begin executing the process illustrated in Figure 10; tester II 902b is ready to begin executing the process illustrated in Figure 11; and each on-line test station 904a-904c is ready to begin executing the process shown in Figure 12.

[0060] As shown in Figure 10, tester I 902a selects a test station at step 1002. The selected test station may be any of the on-line test stations as listed in the main memory 148 of tester I 902a. For purposes of this example, all three of the test stations—test station A 904a, test station B 904b, and test station C 904c—are listed as on-line in the main memory 148 of tester I 902a, and tester I 902a selects test station A 904a at step 1002. At step 1003, tester I 902a sends a message to tester II 902b that test station A 904a is selected. Thereafter, at step 1004, tester I 902a initiates testing on the first die 916a of wafer 914 in test station A 904a. In this example, tester I 902a does so by transmitting wirelessly one or more test vectors to test station A 904a. Step 1004 may also include setting a flag in the main memory 148 of tester I 902a indicating that testing is underway at the selected test station—test station A 904a.

[0061] After initiating testing of die 1 916a of wafer 914 at the selected test station 904a at step 1004, tester I 902a determines at step 1006 whether it has received any messages. If not, tester I 902a selects another of the on-line testers at step 1008, which may be accomplished generally as described above with respect to Figure 4. In this example, tester I 902a selects test station B 904b at step 1008. Tester I 902a then repeats the process of Figure 10 beginning at step 1003. That is, tester I 902a sends a message to tester II 902b that test station B 904b is now selected, and tester I 902a initiates testing of die 1 916a of wafer 914 at the new selected test station—test station B 904b. As this process continues, tester I 902a initiates testing of die 1 916a of all of the wafers 914 in each of the on-line test stations 904, and tester I 902a sends a message to tester II 902b each time one of the test stations is selected.

[0062] Referring now to Figure 11, after initialization, tester II 902b waits for messages at step 1101. In response to a message sent by tester I 902a at step 1003 of Figure 10 identifying a selected test station, tester II 902b initiates testing of die 2 916b of the wafer 914 at the selected test station at step 1109. Like tester I 902a, in this example, tester II 902b initiates testing of die 2 916b by wirelessly transmitting one or more test vectors to the selected test station.

[0063] As should be apparent, the operation of the process of Figure 10 in tester I 902a and the process of Figure 11 in tester II 902b results in the roughly simultaneous initiation of testing of die 1 916a (by tester I 902a) and die 2 916b (by tester II 902b) of the wafer 914 at the selected test station.

[0064] Referring now to Figure 12, after initialization, each test station 904a-904c waits for messages at step 1201. Upon receiving test vectors from one of the testers 902 (sent by tester I 902a at step 1004 of Figure 10 or tester II 902b at step 1109 of Figure 11), the test station 904 writes the test vectors through the probes 912 of probe card 908 (see steps 1206, 1210, 1212). If the test vectors were received from tester I 902a, the test station 904 writes the test vectors to die 1 916a; if the tester vectors were received from tester II 902b, the test station 904 writes the test vectors to die 2 916b. Preferably, the test vectors include both test data and an identification of the probes 912 through which the test data is to be written. The test station 904 then collects response data produced by the dice in response to the test vectors and buffers the response data at step 1211. The test station 904 then sends a message at step 1213 to the tester 902 from which the test vectors were received indicating that the tests are completed.

[0065] Referring again to Figure 10, tester I 902a, upon receiving a message from a test station 904 indicating that testing has completed (see steps 1006, 1010), processes the results of the testing at step 1012, which may include such things as sending a message to the test station 904 requesting transmission of the test results. In this example, wafer 914 must be moved after testing dice 916a, 916b to contact and test dice 916c, 916d. At step 1017, if tester I 902a has received an indication from tester II 902b that testing of die 2 916b has been completed, tester I 902a causes the test station 904 to move the wafer 914 to contact and test dice 916c, 916d.

[0066] Referring now to Figure 11, tester II 902b, upon receiving a message from a test station 904 indicating that the testing has completed (see steps 1106, 1110), tester II 902b processes the results of the testing at step 1112, which may include such things as sending a message to the test station requesting transmission of the test results. At step 1113, tester II 902b sends a message to tester I 902a that testing of die 2 916b has been completed. Referring now to Figure 10, upon receiving such a message from tester II 902b, tester I 902a causes the test station 904 to move the wafer 914 to contact and test dice 916c, 916d if testing of die 1 916a has been completed. (See steps 1007, 1015.)

[0067] Referring again to Figure 12, a test station 904 that receives a message from one of the testers 902a, 902b requesting the results of testing sends the test results to the tester 902 at step 1216 (see also steps 1206, 1214). Element 1218, labeled "other," in Figure 12 represents other tasks that might be performed by a test station 904. Moving the wafer in response to a command

from tester I 902a (as discussed above) is an example of such a task. A message originating from any number of possible sources stopping the process of Figure 12 is another example. Stopping the process and other miscellaneous tasks may be performed at step 1018 in Figure 10 and 1118 in Figure 11.

[0068] As with other processes described above, a new test station may send a messages to tester I 902a requesting to be brought on line. Likewise, an on-line test station may send a message to tester I 902a requesting to be taken off line. Such requests are processed by tester I 902a at steps 1014, 1016 of Figure 10, and may be accomplished in a manner generally similar to step 416 of Figure 4 as described above.

[0069] As mentioned previously, the processes illustrated in Figures 2-5, 7, 8, and 10-12 are exemplary only and not to be taken as limiting. Similarly, the systems shown in Figures 1, 6, and 9 are exemplary only and not to be taken as limiting.

[0070] It should be apparent that, in all of the processes illustrated in Figures 4, 6, and 10, provisions may be made for by passing steps 408, 608, and 1008 if no new test stations are available. Such provisions are, however, well within the skill of a person of ordinary skill in the field and need not be discussed. Similarly, provisions for processing error conditions, exiting the processes illustrated in Figures 2-5, 7, 8, and 10-12, or processing multiple messages are well within the skill of a person of ordinary skill in the field and also need not be discussed.

[0071] Note that probe cards, such as probe card 108 in Figure 1 and probe card 908 in Figure 9, are often capable of contacting many more than one die at a time. Thus, die 116b in Figure 1 may represent a plurality of dice being contacted by probe card 108. Likewise, each of dice 916a and 916b in Figure 9 may represent a plurality of dice being contacted by probe card 908.

[0072] Although specific embodiments and applications of the invention have been described in this specification, there is no intention that the invention be limited to these exemplary embodiments and applications or to the manner in which the exemplary embodiments and applications operate or are described herein.